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EXAMINER

PATEL, NIKETA I

ART UNIT PAPER NUMBER

2182

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/038,231

Applicant(s)

SICOLA ET AL.

Examiner

Niketa I. Patel

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claims 10-21 are objected to because of the following informalities: independent claims 10 and 19 are amended to include the limitation of generating a shelf identifier by the cabinet bus however, the discloser teaches otherwise. At, page 12, lines 8-12 of the specification states "...This is achieved with the use of the cabinet bus 60, 62 that includes a series of junction boxes 66, 68 that each **provide** a unique shelf identifier for a set of shelves 24, 54 (such as for 2 shelves.)" (Emphases added) The Examiner has carefully reviewed pages 12-17 and concludes that this citation teaches that the bus is used to provide a shelf identifier signal rather than generating a shelf identifier signal. Furthermore, by definition bus is a carrier of a signal not a generator of the signal.

Claims 9-18 depend from claim 10 and claims 20-21 depend from claim 19, therefore they inherited the same deficiency. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless -

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 10-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Martinez et al. U.S. Patent Number: 5,790,782 (hereinafter referred to as "Martinez '782".)

4. Referring to claim 10, Martinez '782 teaches, a cabinet for physically storing and communicatively linking computing devices, comprising: a plurality of shelves adapted for receiving device enclosures [see figure 1 - elements 1-4]; a cabinet bus linked to each of the shelves and adapted to generate and provide a unique shelf identifier signal to each of the shelves [see figure 1 - element 17, 18; column 1 - lines 55-60; column 2 - lines 33-44; see figure 6 - element 17; column 5 - lines 39-57]; and means for providing information identifying the cabinet to each of the shelves [see figure 1 - element 19, 18.]

5. Referring to claim 11, Martinez '782 teaches, further including a device enclosure on one of the shelves comprising processor for processing the unique shelf identifier to determine a physical location within the cabinet [see column 5 - lines 28-44, 'EMU'.]

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6. Referring to claim 12, Martinez '782 teaches, that the processor includes the determined physical location and the cabinet identification information in message transmitted outside the enclosure [see column 5 - lines 28-67; column 6 - lines 1-31.]

7. Referring to claim 13, Martinez '782 teaches, that the processor determines the physical location by retrieving a shelf identifier from memory using the received shelf identifier signal [see column 1 - lines 64-67; column 2 - lines 1-34; column 5 - lines 65-67.]

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 14 and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Martinez et al. U.S. Patent Number: 5,790,782 (hereinafter referred to as "Martinez '782".)

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10. **Referring to claim 14**, *Martinez '782* as modified by the teachings of *Martinez '665* above teaches, that the received shelf identifier signal is a 5-bit signal, however fails to teach that the received shelf identifier signal is an 8-bit signal.

Martinez discloses that the 5-bit signal is an example, not to be taken as a limitation on the spirit and scope of this invention [see column 9 - lines 15-23.]

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well known in the computer art to get the advantage of being able to address greater number of elements with a higher bit signal. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to include a higher bit signal to get this advantage.

11. **Referring to claim 19**, *Martinez '782* as modified by the teachings of *Martinez '665* above, teaches a data storage system with passive position determination of enclosures, comprising: a cabinet having a plurality of shelves for receiving and linking computing devices [see figure 1 - elements 1-4], a cabinet bus linked to the shelves for generating and providing a shelf identifier to each shelf [see figure 1 - element 17], and a device for providing a cabinet identifier to each shelf [see figure 1 - elements 15, 16]; a device enclosure positioned on

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one of the shelves in one of the cabinets and linked to the cabinet bus in the one cabinet, wherein the device enclosure receives the shelf identifier for the one shelf and the cabinet identifier for the one cabinet and creates and transmits a physical location message [see column 1 - lines 55-67; column 2 - lines 1-44]; and a host linked to the one cabinet receiving the physical location message and outputting a physical location of the device enclosure including the one shelf and the one cabinet [see figure 5 - element 30], however fails to teach a plurality of cabinets containing above elements.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well known in the computer art to get the advantage of having plurality of storage locations to hold multiple enclosures by using plurality of cabinets. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to include a plurality of cabinets to get this advantage.

12. Claims 1-9, 15-18 and 20-21 are rejected under 35 U.S.C. 103(a) as being obvious over Martinez et al. U.S. Patent Number: 5,790,782 (hereinafter referred to as "*Martinez* '782") and

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further in view of Martinez et al. U.S. Patent Number: 5,956,665 (hereinafter referred to as "*Martinez '665*".)

13. **Referring to claim 1**, *Martinez '782* teaches a position sensing apparatus for use in a data storage cabinet having multiple shelves for receiving device enclosures [see column 1 - lines 38-49], comprising: a first connector having an output connection at a first shelf of the cabinet for providing a first shelf identifier signal to a device enclosure connected to the first shelf [see figure 1 - element 15; column 4 - lines 8-33, 'connector']; and a second connector linked to the first connector [see figure 1 - element 15, 16, 17] for receiving an output signal and having an output connection at a second shelf of the cabinet for providing a second shelf identifier signal to a device enclosure connected to the second shelf, wherein the second shelf identifier signal differs from the first shelf identifier signal [see column 1 - lines 55-60; column 2 - lines 33-44; see figure 6 - element 17; column 5 - lines 39-57.]

Martinez '782 does not set forth the limitation of the first connector and the second connector being junction boxes, however *Martinez '665* teaches a use of junction box [see *Martinez '665* column 6 - lines 42-62, 'upper jack and lower jack'] in order to connect two shelves and provide a level of redundancy in the event of a failure in one of the shelf-to-shelf cables.

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One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous to use junction box as the connectors of *Martinez*'782 in order to provide a level of redundancy in the event of a failure in one of the shelf-to-shelf cables. It is for this reason that one of ordinary skill in the art would have been motivated to substitute *Martinez*'782 connectors with a junction boxes to provide a level of redundancy in the event of a failure in one of the shelf-to-shelf cables.

14. **Referring to claim 2**, *Martinez*'782 as modified by the teachings of *Martinez*'665 above teaches, that the first and second junction boxes each include an additional output connection at third and fourth shelves of the cabinet for providing third and fourth shelves of the cabinet for providing third and fourth shelf identifier signals differing from the first and second shelf identifier signals, respectively [see figure 1 - element 11, 16, 15, 12-14; column 2 - lines 33-44; column 5 - lines 39-57.]

15. **Referring to claim 3**, *Martinez*'782 as modified by the teachings of *Martinez*'665 above teaches, that each of the junction boxes includes a sensing wire providing signals to the output connections and being alternately grounded and open to differentiate the first and second shelf identifier signals from

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the third and fourth shelf identifier signals [see figure 6 - element 43, 35.]

16. **Referring to claim 4, Martinez '782** as modified by the teachings of *Martinez '665* above teaches, that the junction boxes include a first and a second set of sensing wires each providing a number of bit signals that are included in the shelf identifier signals to the output connections [see figure 6 - elements 38, 37, 41, 44.]

17. **Referring to claims 5-6 and 18, Martinez '782** as modified by the teachings of *Martinez '665* above teaches, that the number of signals is based on the number of wires in each of the sets [see column 5 - lines 40-57] however, fails to teach that the number of wires in the first set differs from the number in the second set and that the number of wires in the first set is three and the number of wires in the second set is four, to provide at least 24 of the unique shelf identifier signals wires to provide at least 24 of the unique shelf identifier signals within the cabinet bus.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well known in the computer art to get the advantage of being able to address grater number of elements with a higher bit signal and lesser number of elements with a smaller bit signal.

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It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to include a higher/smaller bit signal to get this advantage.

18. **Referring to claim 7, Martinez '782** as modified by the teachings of *Martinez '665* above teaches, that the sensing wires of the first and second sets are passed through the first junction box and are included in the output signal to the second junction box and further wherein each of the sensing wires in the first set are moved one position within the first set and each of the sending wires in the second set are moved one position within the second set prior to the link with the second junction box [see column 5 - lines 39-67; column 6 - lines 1-34.]

19. **Referring to claim 8, Martinez '782** as modified by the teachings of *Martinez '665* above teaches, that the first junction box and the second junction box are interchangeable [see figure 1 - elements 15, 16.]

20. **Referring to claim 9, Martinez '782** as modified by the teachings of *Martinez '665* above teaches, that including a cabinet area network bus having terminating resistors at each end [see figure 6 - elements 43, 35, 'resisters'.]

21. **Referring to claim 15, Martinez '782** teaches that the cabinet bus comprises a plurality of serially connected

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connectors each including a first set of sensing and a second set of sensing wires and a side connector linked to one of the shelves for providing the shelf identifier signal from the first and second sets of sensing wires [see figure 1 - elements 15, 16, 17, 11-14.] *Martinez*'782 does not set forth the limitation of the first connector and the second connector being junction boxes, however *Martinez*'665 teaches a use of junction box [see *Martinez*'665 column 6 - lines 42-62, 'upper jack and lower jack'] in order to connect two shelves and provide a level of redundancy in the event of a failure in one of the shelf-to-shelf cables.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous to use junction box as the connectors of *Martinez*'782 in order to provide a level of redundancy in the event of a failure in one of the shelf-to-shelf cables. It is for this reason that one of ordinary skill in the art would have been motivated to substitute *Martinez*'782 connectors with a junction boxes to provide a level of redundancy in the event of a failure in one of the shelf-to-shelf cables.

22. **Referring to claim 16**, *Martinez*'782 as modified by the teachings of *Martinez*'665 and applied to claim 15 above, teaches that each of the sensing wires in the first set are moved one

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position and each of the sensing wires in the second set are moved one position prior to the connection to an adjacent junction box to provide an output signal to modify the shelf identifier signal in each consecutive junction box in the cabinet bus [see column 5 - lines 28-67; column 6 - lines 1-31.]

23. **Referring to claim 17**, *Martinez '782* as modified by the teachings of *Martinez '665* and applied to claim 15 above, teaches that each junction box further includes an additional side connector linked to the first and second sets of sensing wires and an additional sensing wire that is linked to the side connectors and is alternately grounded and ungrounded at each side connector to provide differing one of the shelf identifier signals within each junction box [see figure 6 - elements 35, 43; column 5 - lines 28-67; column 6 - lines 1-31.]

24. **Referring to claim 20**, *Martinez '782* teaches that the cabinet bus includes a plurality of connectors comprising a first and second set of sensing wires linked to the shelves and carrying the shelf identifier [see figure 1 - elements 15, 16], the sensing wires of the first set rotating one position within the first set prior to connection to the next one of the connectors and the sensing wires of the second set rotating one position within the second set prior to connection to the next one of the connectors, whereby the shelf identifier output to

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the next one of the connectors is modified [see column 5 - lines 28-67; column 6 - lines 1-31.] *Martinez*'782 does not set forth the limitation of the first connector and the second connector being junction boxes, however *Martinez*'665 teaches a use of junction box [see *Martinez*'665 column 6 - lines 42-62, 'upper jack and lower jack'] in order to connect two shelves and provide a level of redundancy in the event of a failure in one of the shelf-to-shelf cables.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous to use junction box as the connectors of *Martinez*'782 in order to provide a level of redundancy in the event of a failure in one of the shelf-to-shelf cables. It is for this reason that one of ordinary skill in the art would have been motivated to substitute *Martinez*'782 connectors with a junction boxes to provide a level of redundancy in the event of a failure in one of the shelf-to-shelf cables.

25. **Referring to claim 21**, *Martinez*'782 as modified by the teachings of *Martinez*'665 and applied to claim 20 above, teaches that each of the junction boxes is connected to two shelves and the cabinet bus further includes an additional sensing line that is grounded prior to a first one of the two shelves and is ungrounded prior to a second one of the two shelves [see figure

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1 - elements 15, 16, 17, 11-14; figure 6 - element 35, 43;
column 6 - lines 47-59.]

Response to Arguments

26. Applicant's arguments filed 09/08/2004 have been fully considered but they are not persuasive.

The applicant argues that prior art cited by the Examiner does not teach a cabinet bus that generates and provides a unique shelf identifier signal (see pages 6-8.)

The Examiner respectfully disagrees with this argument. At, column 5, lines 40-57 *Martinez* '782 teaches input connectors and a cable, which provides an analog voltage, whose analog magnitude comprises the decimal equivalent of the binary values, which is a shelf address, i.e., a unique shelf identifier. The Examiner has carefully reviewed pages 12-17 of the specification and concludes that this citation teaches that the bus is used to provide a shelf identifier signal rather than generating a shelf identifier signal. The apparatus of *Martinez* '782 operates in the same manner as the applicant's apparatus as cited on pages 12-17. The only clear difference is that the *Martinez* '782 teaches an analog unique shelf identifier signal and the applicant discloses a digital unique shelf identifier signal, however the claim language does not exclude an analog signal.

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Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (571) 272 4156. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (571) 272 4146. The fax phone number for the

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organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP
11/22/2004



KIM HUYNH
PRIMARY EXAMINER

11/24/04